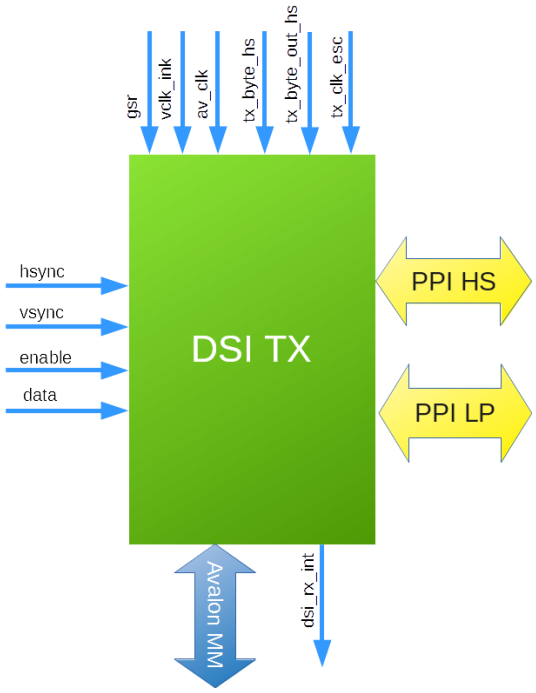
IQ-DSI-Tx

MIPI(r) DSI Transmitter IP Core



Core Facts	
Core specifics	
Supported Device Family	MAX 10
Supported User Interfaces	PPI, AVALON MM
Provided with Core	
Documentation	User's Manual
Design Files	VHDL
Example design	VHDL
Test bench	VHDL
Constraints File	Timing
Simulation tool used	
Modelsim Intel FPGA edition	
Support	
Support Provided by Mikroprojekt d.o.o	

IQ-DSI-Tx is a MIPI DSI protocol engine/ transmitter IP core designed to work with PPI-compatible MIPI D-PHY serial interfaces for driving embedded displays.

Features

- Programmable number of serial data lanes (1-4)
- Data rate from 80 to 900 Mbps per lane
- PHY-Protocol Interface (PPI) towards D-PHY
- Clocked video interface at input
- HS (High Speed) mode transmission support
- Transmit and receive (bus turnaround) in LP (Low Power) mode
- Supports all DSI compatible video formats
- Video modes support (Non-burst with sync pulses, Non-burst with sync events, Burst mode)
- Register accessible command queue for transmission of command packets in HS Blank or LP mode
- Programmable EoTp generation
- ECC generation for header
- CRC generation for packet payload
- Avalon-MM interface for register access
- Compliant to MIPI Alliance Specification for Display Serial Interface v1.3.1

Unsupported Features

- DSI Video command mode
- DSI Virtual channels

Core utilization

DEVICE	LE	REG	M9K	I/O
MAX 10	1906	1167	18	N/A

Ordering information

Please contact us via email **contact@mikroprojekt.hr** about item availability and ordering details.